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Global trigger for the DarkSide 50 experiment

The DAQ system of the DarkSide 50 experiment includes TPC digitizers and Veto digitizers. The TPC DAQ uses CAEN v1720 modules and the Veto system uses NI PXIe-5162 modules. The main difference between two digitizers is the width of the selected data acquisition window. For the PXIe-5162 it is between 1 uS and 60 uS, while for the v1720 it is about 300 uS. It is highly desirable to synchronize two types of the digitizers with the TPC trigger, so full background information is available for each TPC event. At the time of this writing there is no information available at National Instruments web site on the PXIe-5162 digitizer. It is assumed below that this digitizer behaves similarly to the CAEN v1720 in terms of event buffering and triggers overlap.

The following scheme is proposed to satisfy the above synchronization requirement. The Hardware Veto Trigger signals are sent via optical links to the v1495 trigger module located at the TPC site. Currently there are two types of Hardware Veto triggers: Scintillation Counter (SC) trigger and Cherenkov Water detector (CW) trigger. The v1495 module generates *all the triggers* for the experiment. The Veto trigger and 16-bit Trigger ID are transferred via optical link back to another v1495 module located at the Veto system site. The trigger ID consists of two parts: 12-bit Trigger Number and 4-bit Trigger Type. The v1495 logic decodes the Trigger ID and places it in an internal FIFO memory for the readout via VME bus as a part of the TPC data stream. The same Trigger ID and the trigger signal are also available for the Veto DAQ readout via digital adapter module NI 6583 attached to FlexRIO FPGA PXIe-7961R module. The FlexRIO FPGA PXIe-7961R module is similar to the CAEN v1495 module and allows user to implement desirable trigger logic in on-board FPGA. The depth of the FIFO memory for storing Trigger ID information has to match the number of buffers allocated in the flash ADCs in each DAQ sub-system. A 50 MHz clock signal is also sent to the Veto site for synchronization of both Veto and TPC ADCs to the same clock frequency. Both v1495s also receive the 1PPS signal from the LNGS GPS receiver.

The triggers arriving at v1495 located at the Veto site are dedicated for the Veto digitizers and TDCs. A separate trigger signal (TPC trigger) required for the TDC modules located at the Veto site can be implemented using Trigger Type bits of the Trigger ID. In order to manage high trigger rates, the Memory Full signals of the v1720 ADCs are ORed and used to inhibit TPC triggers when there are no memory buffers available. A similar Memory Full signal has to be derived by the FlexRIO FPGA PXIe-7961R module in the Veto DAQ system in order to keep data readout rate at the maximum. This signal is sent to the TPC site to prevent generation of the TPC trigger (and associated Veto triggers) when the Veto system is busy. Optionally this signal could also be used locally to block Hardware Veto triggers (dashed line). The FlexRIO FPGA PXIe-7961R module has internal memory which can be used as a FIFO to

store Trigger ID for each incoming Veto trigger. This memory has to be read out with each event in order to provide a marker for event synchronization.

The main trigger unit has to generate appropriate dead time for each trigger type equal to the data acquisition window to prevent trigger overlap within it. In addition, the TPC trigger will not be issued, if the Veto trigger processing (1 to 60 uS) is in progress. The Veto triggers will be generated at the desired rate and each Veto trigger type will have a unique Trigger Number. The main trigger unit will increment the Trigger Number when any trigger type is generated. When the TPC trigger is generated, the Trigger Number sent to the Veto system with each trigger will not be incremented within 300 uS of the TPC data acquisition window. This will mark all Veto events within that window with the *same Trigger Number* (but different Trigger Type) and will allow easy event synchronization. Additionally, the lower eight bits of the Trigger Number are sent to the v1720 I/O connectors. This 8-bit number is called TPC Trigger Ordinal. Details of the trigger logic will be developed after this proposal is approved by DS 50 experiment.

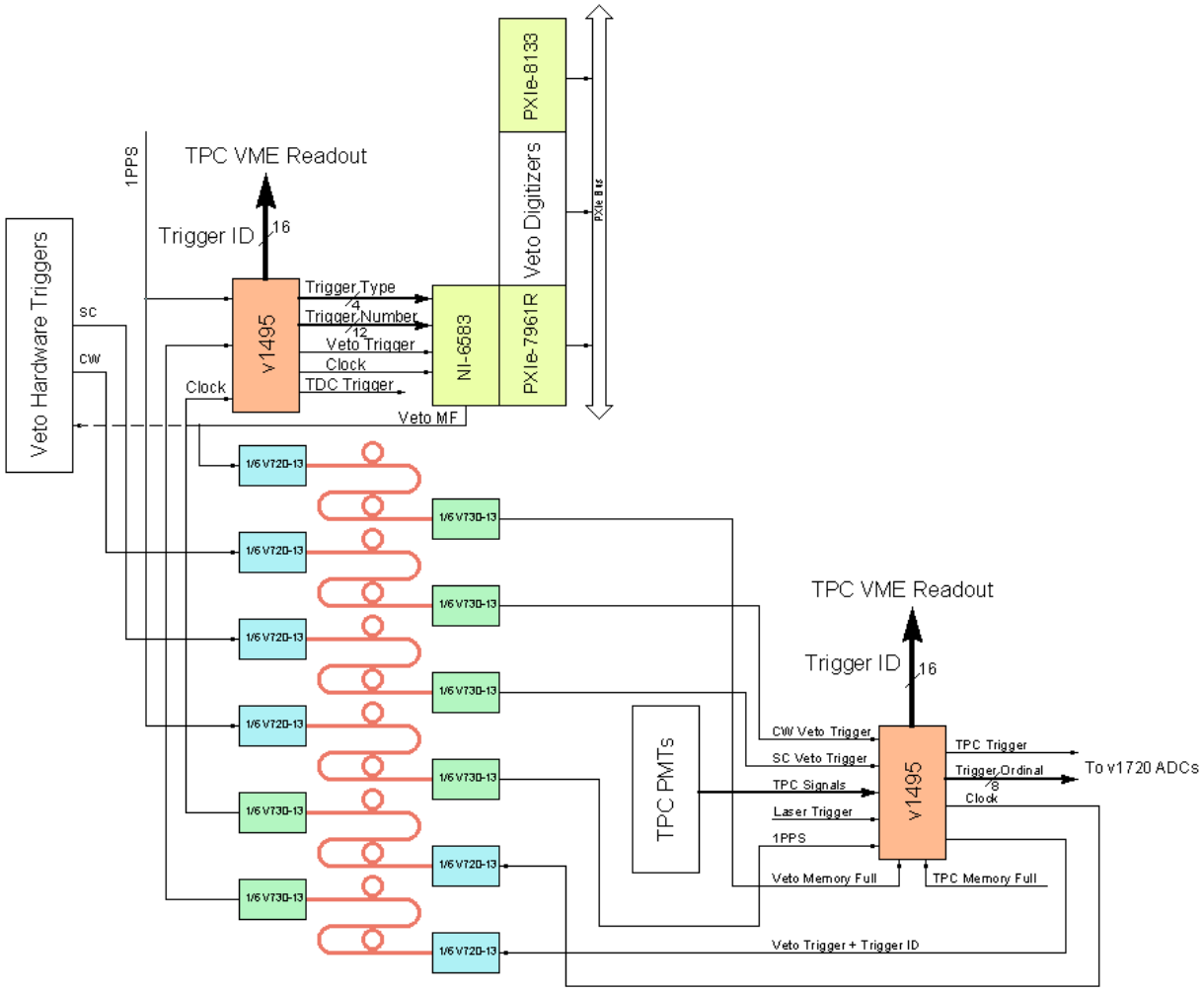

Figure 1. Block-diagram of the proposed DS 50 global trigger system